I3 Background Spatial Variation: 0.3-0.7 keV

phase all: [CCD 3] 0.300–0.700 keV
Background Spatial Variation (ACIS “stowed”)
FI Chips – example I3

I3 Background Spatial Variation: 1.0-2.0 keV

phase all: [CCD 3] 1.000–2.000 keV
Background Spatial Variation (ACIS “stowed”)  
FI Chips – example I3

I3 Background Spatial Variation: 2.0-5.0 keV

phase all: [CCD 3] 2.000–5.000 keV

![Diagram showing background spatial variation for ACIS I3 chips.](image)
I3 Background Spatial Variation: 5.0-10.0 keV

phase all: \([\text{CCD 3}] 5.000-10.000 \text{ keV}\)
Background Spatial Variation (ACIS “stowed”)
BI Chip – S3

S3 Background Spatial Variation: 0.3-0.7 keV

phase all: \[ [CCD \, 7] \, 0.300-0.700 \, \text{keV} \]
S3 Background Spatial Variation: 1.0-2.0 keV

phase all: [CCD 7] 1.000–2.000 keV
Background Spatial Variation (ACIS “stowed”)
BI Chip – S3

S3 Background Spatial Variation: 2.0-5.0 keV

phase all: [CCD 7] 2.000–5.000 keV

[Graphs and plots showing background variation]

T. Gaetz (CXC/SAO)
Background Spatial Variation (ACIS “stowed”)
BI Chip – S3

S3 Background Spatial Variation: 5.0-10.0 keV

phase all: [CCD 7] 5.000–10.000 keV

![Graphs showing background variation](image-url)
S1 Background Spatial Variation: 0.3-0.7 keV

phase all: [CCD 5] 0.300–0.700 keV