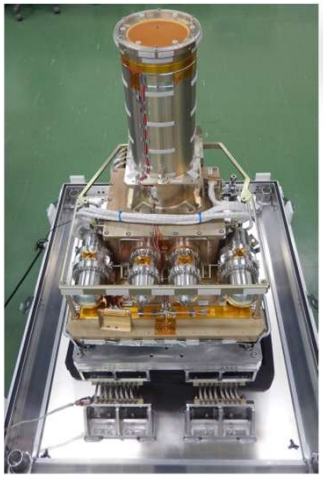
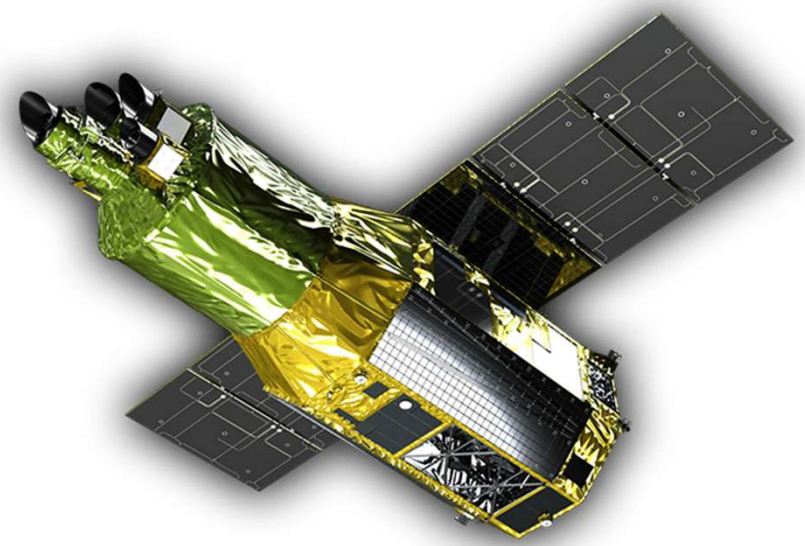
Characterization and calibration of the front-end ASIC for the X-ray CCD camera aboard the XRISM satellite

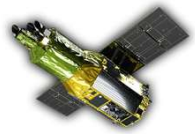




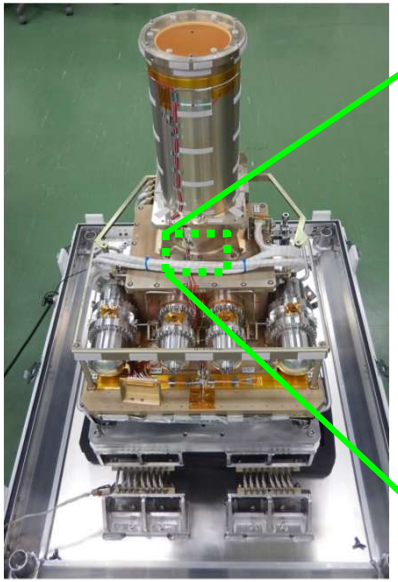
Hikari Kashimura, Hiroshi Nakajima
(Kanto Gakuin University),
Hiroshi Tomida, Yoshitaka Arai (ISAS/JAXA),

Kiyoshi Hayashida, Hironori Matsumoto, Hiroshi Tsunemi, Junichi Iwagaki, Koki Okazaki,
Kazunori Asakura, Tomokage Yoneyema (Osaka University), John P. Doty (Noqsi Aerospace Ltd.),
Hiroyuki Uchida, Takaaki Tanaka, Takeshi G. Tsuru, Hiromichi Okon, Yuki Amano (Kyoto University),
Masanobu Ozaki, Tadayasu Dotani, Hirokazu Ikeda, Takeo Shimoi (ISAS/JAXA),
Koji Mori, Yusuke Nishioka, Ayaki Takeda, Makoto Yamauchi, Isamu Hatsukade, Yoshiaki Kanemaru, Jin Sato (University of Miyazaki),
Takayoshi Kohmura, Kohichi Hagino (Tokyo University of Science), Hiroshi Murakami (Tohoku Gakuin University),
Shogo B. Kobayashi (Tokyo University of Science), Masayoshi Nobukawa (Nara University of Education),
Kumiko K. Nobukawa (Nara Women's University), Junko S. Hiraga (Kwansei Gakuin University),
Hideki Uchiyama (Shizuoka University), Kazutaka Yamaoka (Nagoya University), and the XRISM Xtend team

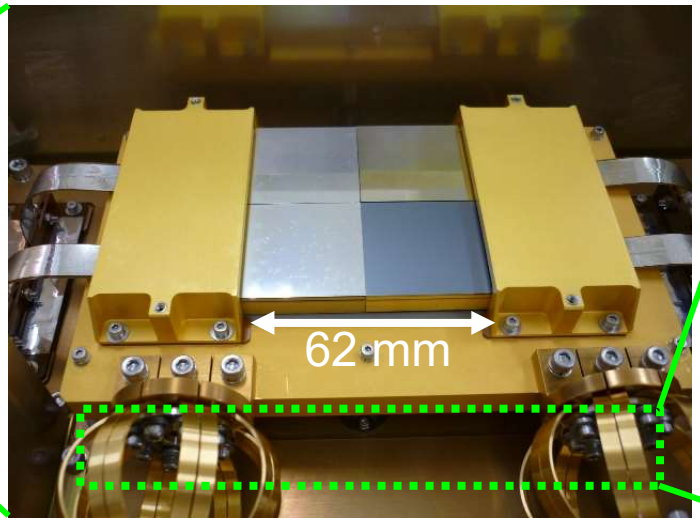
Front-end ASIC for Xtend



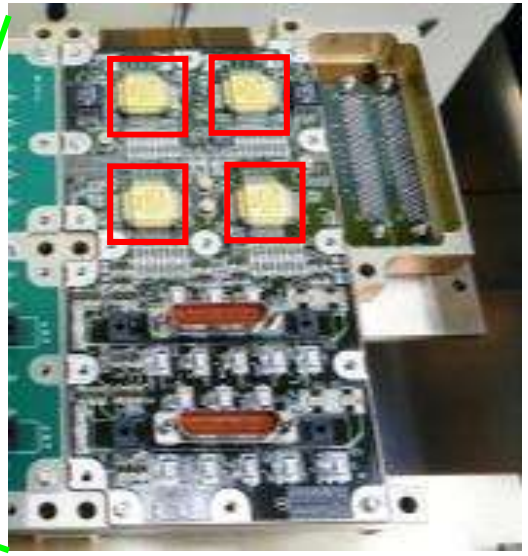
Sensor Body of SXI
(Hitomi FM)



X-ray CCDs on the cold plate

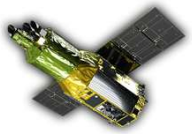


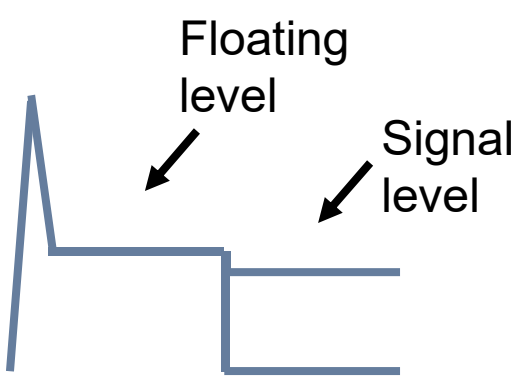
Video Board
under the cold plate

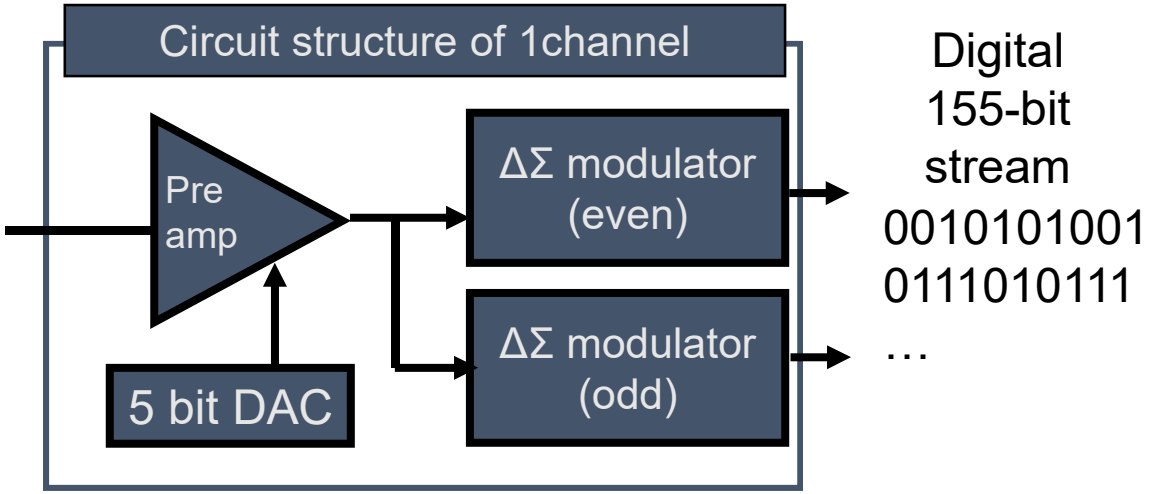


- Sensor body is physically divided into two: one for CCD and another for Video Board that performs front-end signal processing (Tanaka+18)
- Analog signals from CCD are fed to the fully customized ASICs implemented on the Video Board
- Only AC coupling capacitors are between CCD and ASIC, which minimize the distance between them for better noise performance

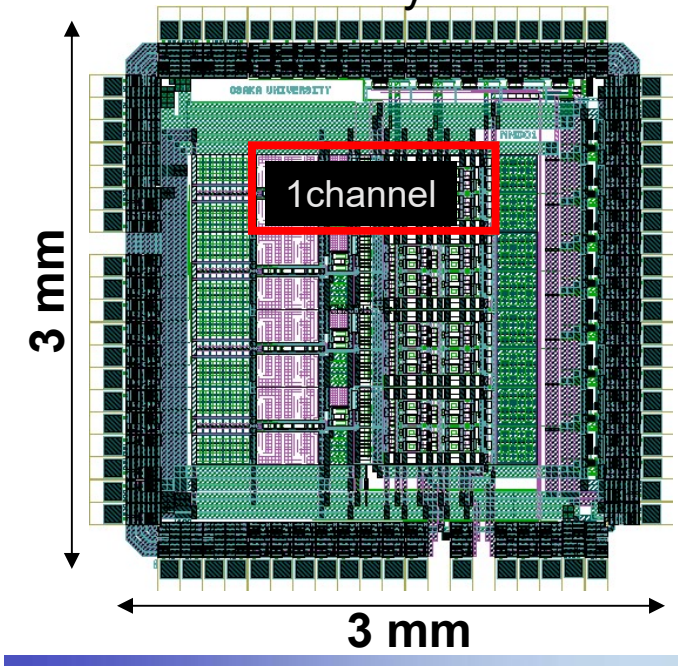
Circuit structure of the ASIC







Mask layout



Pre-amp multiply signal 10 times

DAC gives offset to signal level

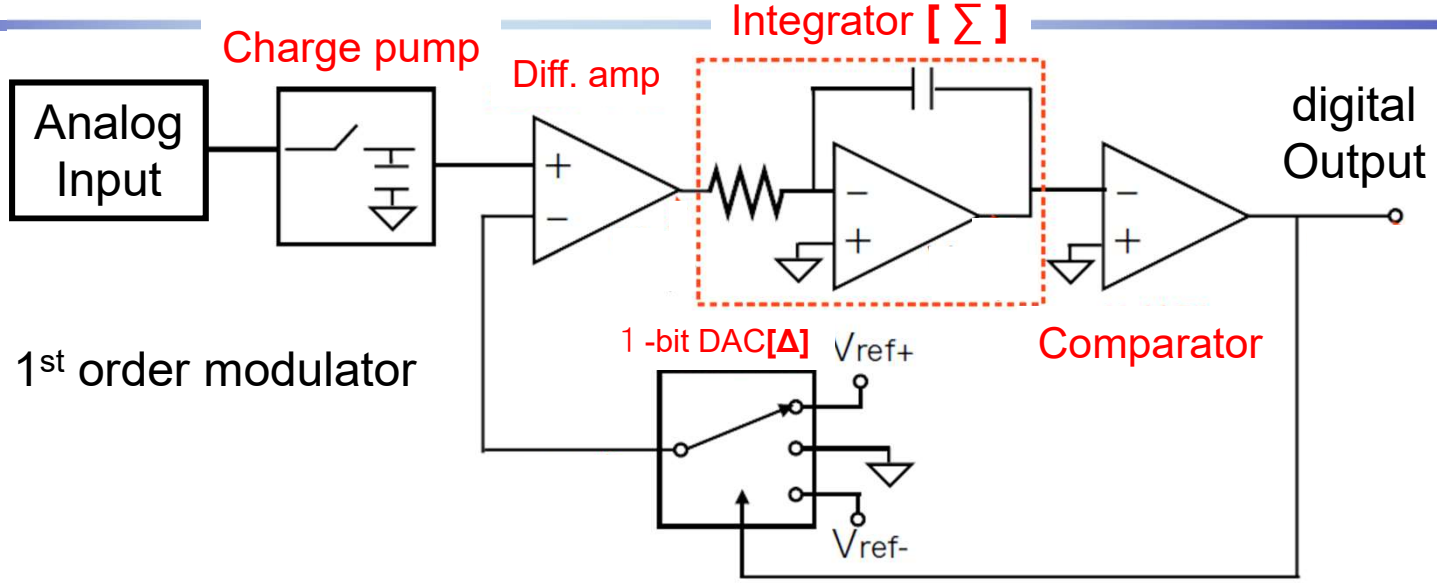
ΔΣ AD conversion of voltage gap

Bare chip size	**3 mm X 3 mm**
Num. of ch	**4**
Power supply	**3.3 V**
process	**TSMC 0.35 μm CMOS**

※made by TSMC via MOSIS service

QFP package of 15mmX15mm

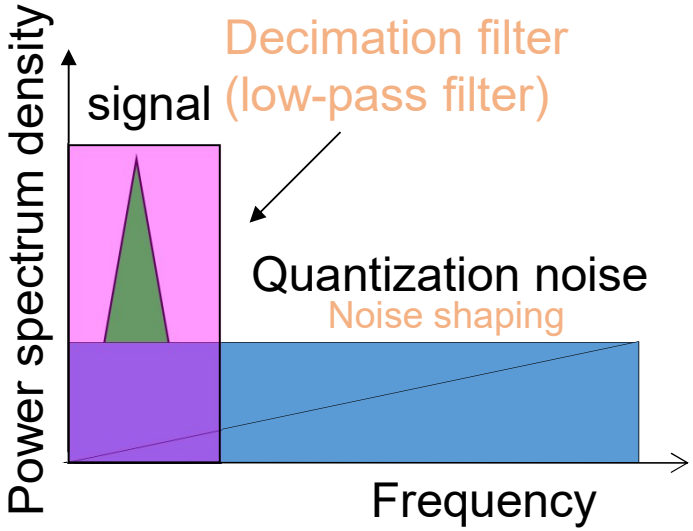
Configuration of ΔΣ modulator



1st order modulator

$$O(f) \approx e^{-j2\pi f T_{clk}} I(f) + 2\pi f T_{clk} N(f)$$

Filter in order to cut the high-frequency quantization noise



x(n) : n-th output
w(n): filter coeff.

ASIC output
0010101001
0111010111
...

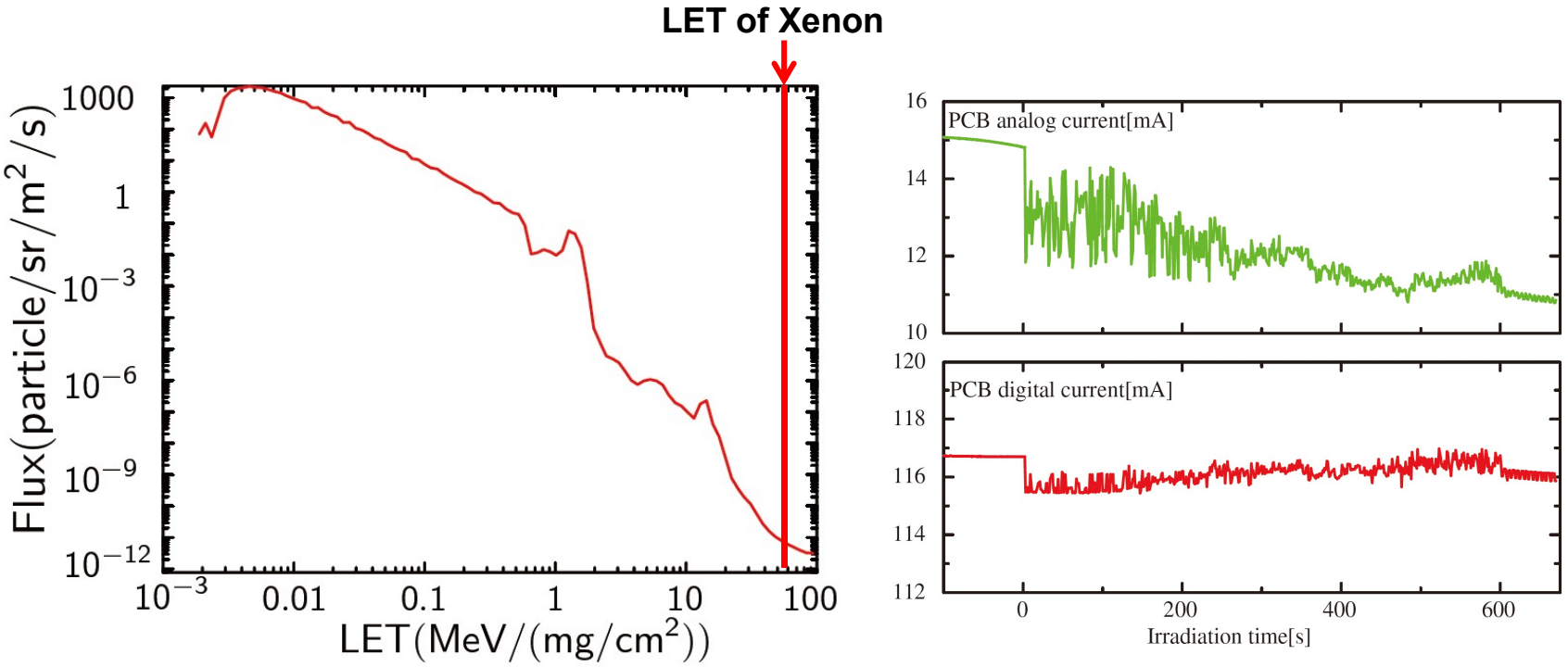
Decimation filter

$$\sum_{n=1}^{n=155} (2 \times x(n) - 1) \times w(n)$$

$$= -w(1) - w(2) + w(3) - w(4) \cdots$$

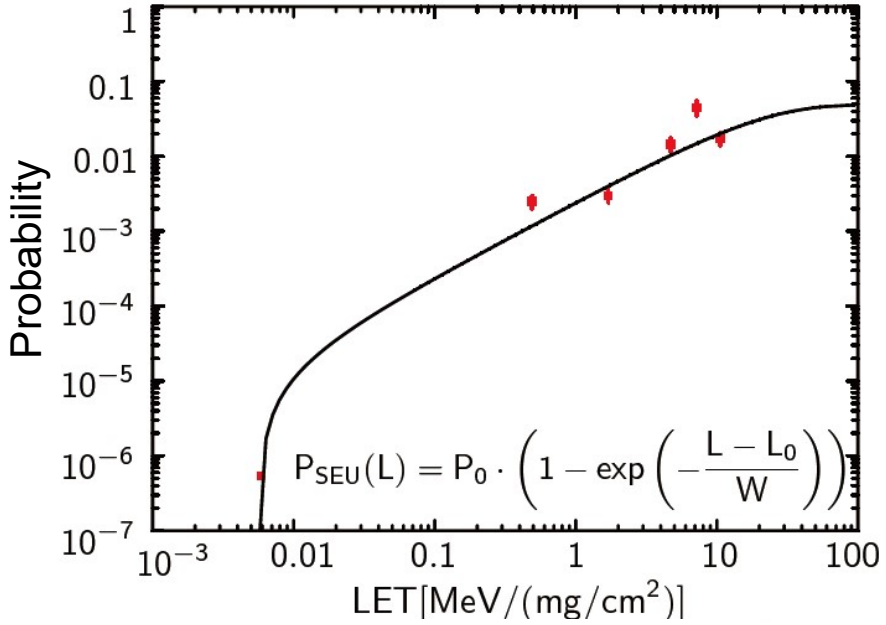
→ decimal value

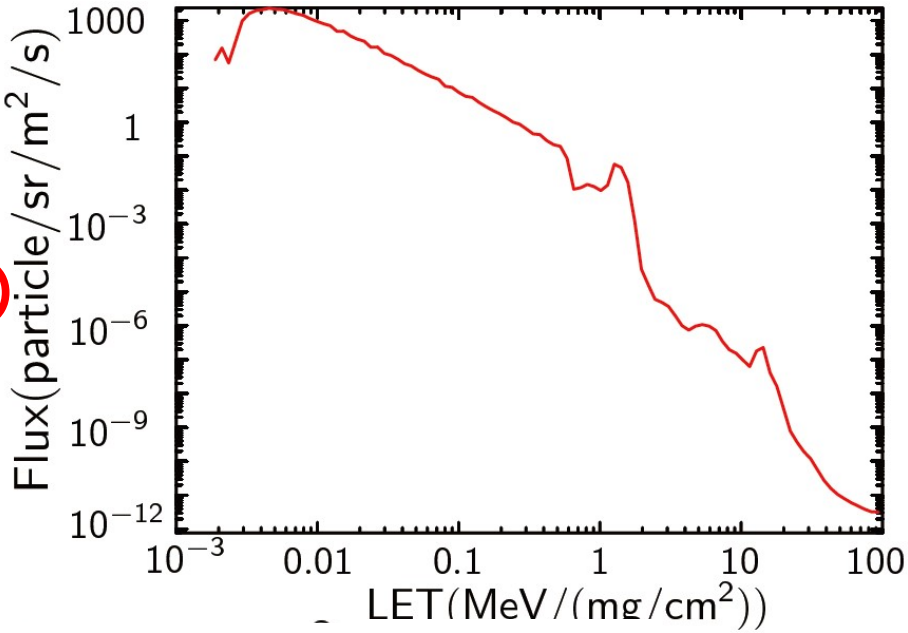
Latch-up tolerance



- Tolerance against single event latch-up (SEL) has been evaluated using Xenon beam with high LET (linear energy transfer) of 57.9 [MeV • cm^2/mg].
- SEL rate is calculated to be once per almost 50 years, which ensures latch-up immunity throughout the mission (Nakajima+13).

Upset tolerance

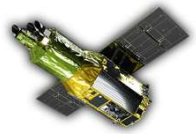




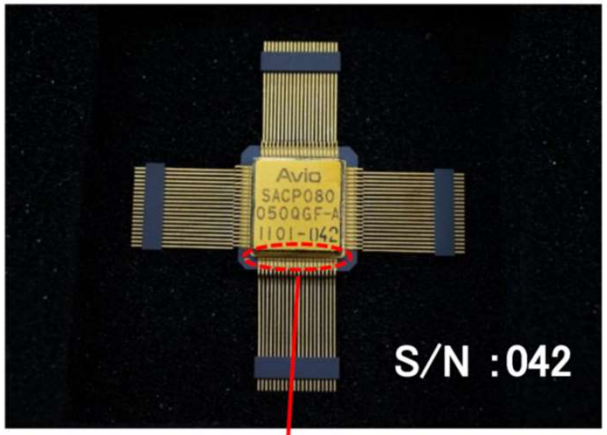
$$R_{SEU} = \int_{L_{th}}^{\infty} \underbrace{F(L)}_{\text{Flux}} \times P_{SEU} \times \underbrace{S}_{\text{Area}} \times \underbrace{\Omega}_{\text{Solid angle}} dL$$

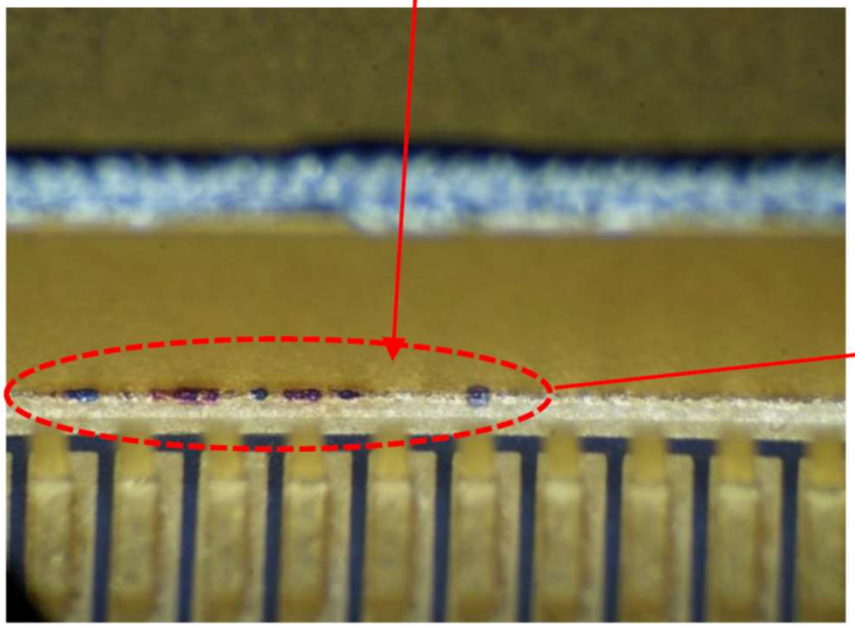
- Estimated SEU (single event upset) event rate in the LEO (height of 550km, inclination angle of 30°): <1.3×10^{-3} events/sec
- This is far smaller than sky X-ray background rate of Hitomi/SXI, which verifies sufficient SEU tolerance
- TID tolerance up to 200krad has been also verified (Nakajima+2011)

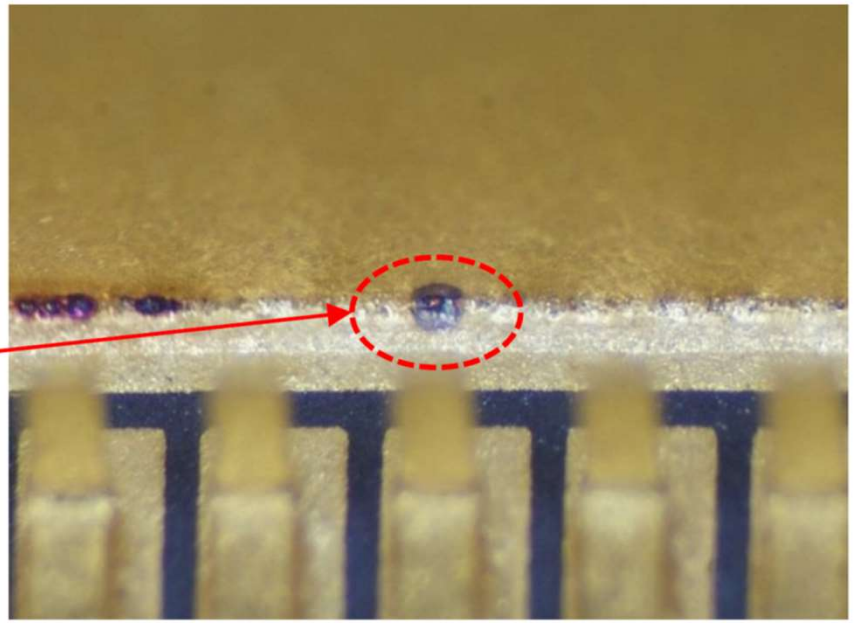
Status of custom package



- We will reuse 8 chips that was fabricated for Hitomi in 2011
- 23 chips had been stored in a desiccator for several years
- Visual inspection by manufacturer said that many of the chips (14/23) had been discolored on the plated surface
- Remaining 9 chips are primary FM candidates

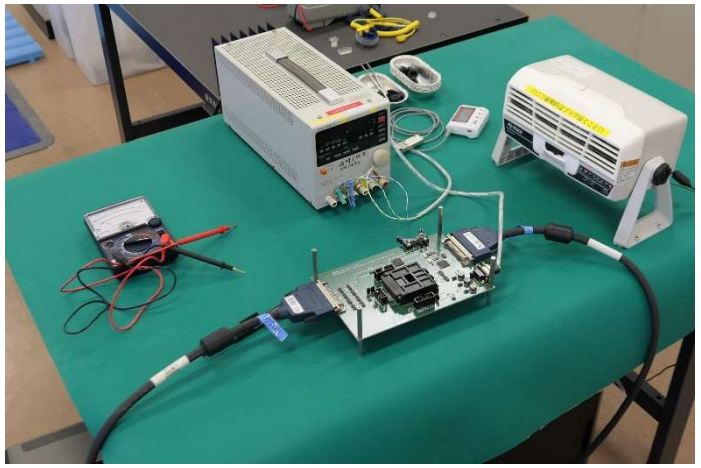


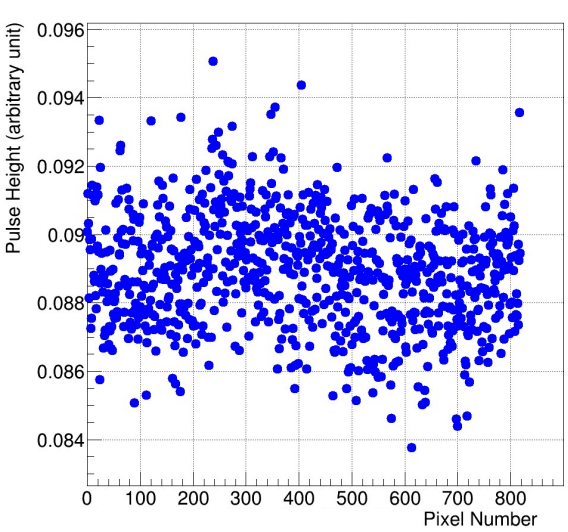


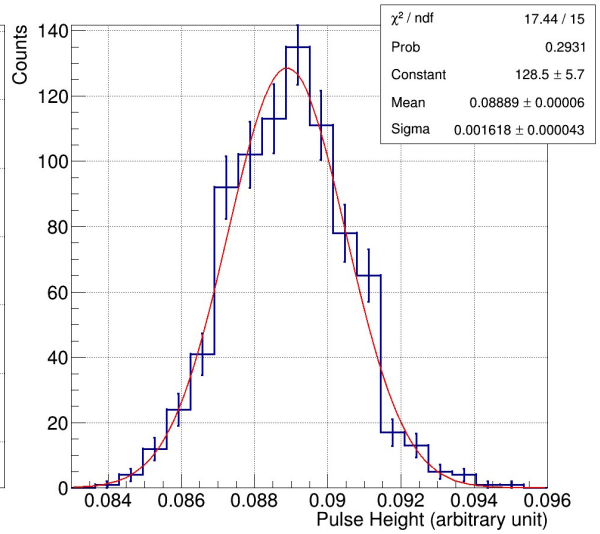


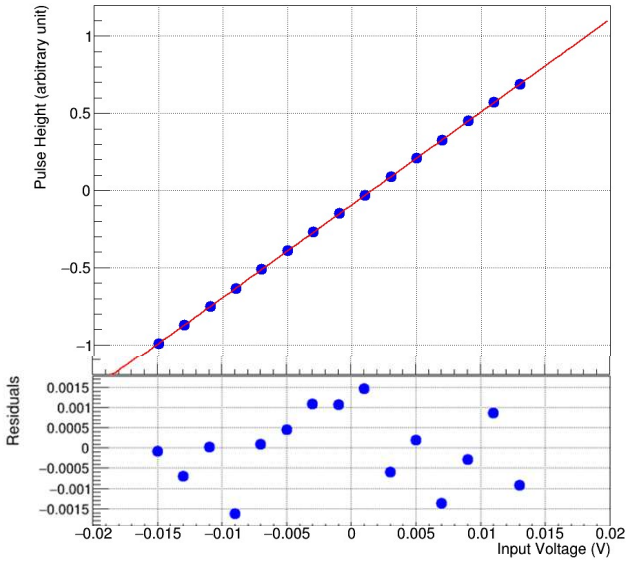
Noise performance

- Performance test has been performed for all 23 chips
- Pseudo CCD signals (∼800 pixels for each input voltage) are processed throughout the dynamic range to evaluate input equivalent noise (IEN), integral non-linearity (INL), and gain







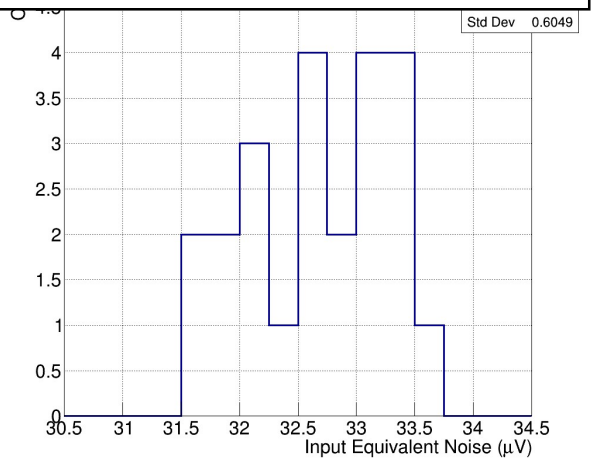


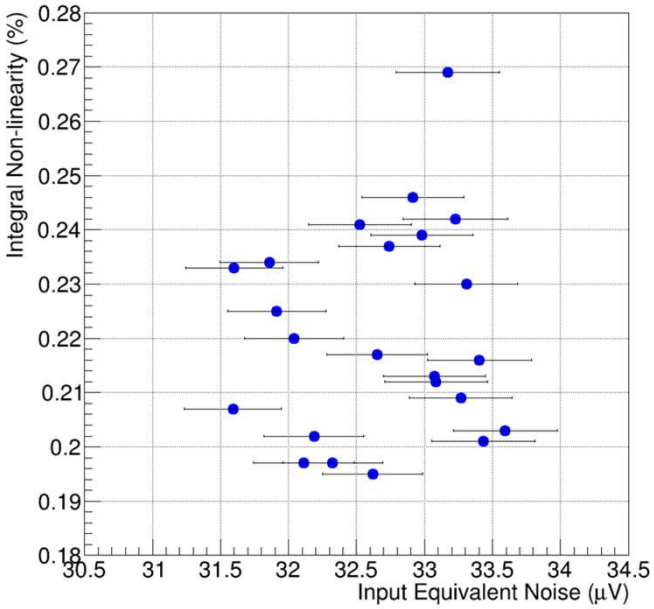
ASIC performance

- All 23 chips showed almost the same performances as those we obtained in 2013
- IEN of ~33μV corresponds to noise level of 6.6e^- (CCD gain is 5μV/e^- typ.)
- Input range of 28mV corresponds to effective energy range of 20.4keV
- All chips passed airtightness tests by manufacturer. Then we will choose FM chips considering both of performance and inspection test results

2019 IEN=32.7±0.6μV

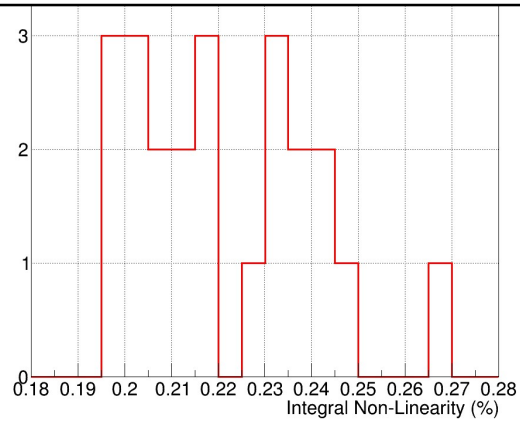
c.f. 2013 IEN=32.7±0.8μV





2019 INL=0.22±0.02%

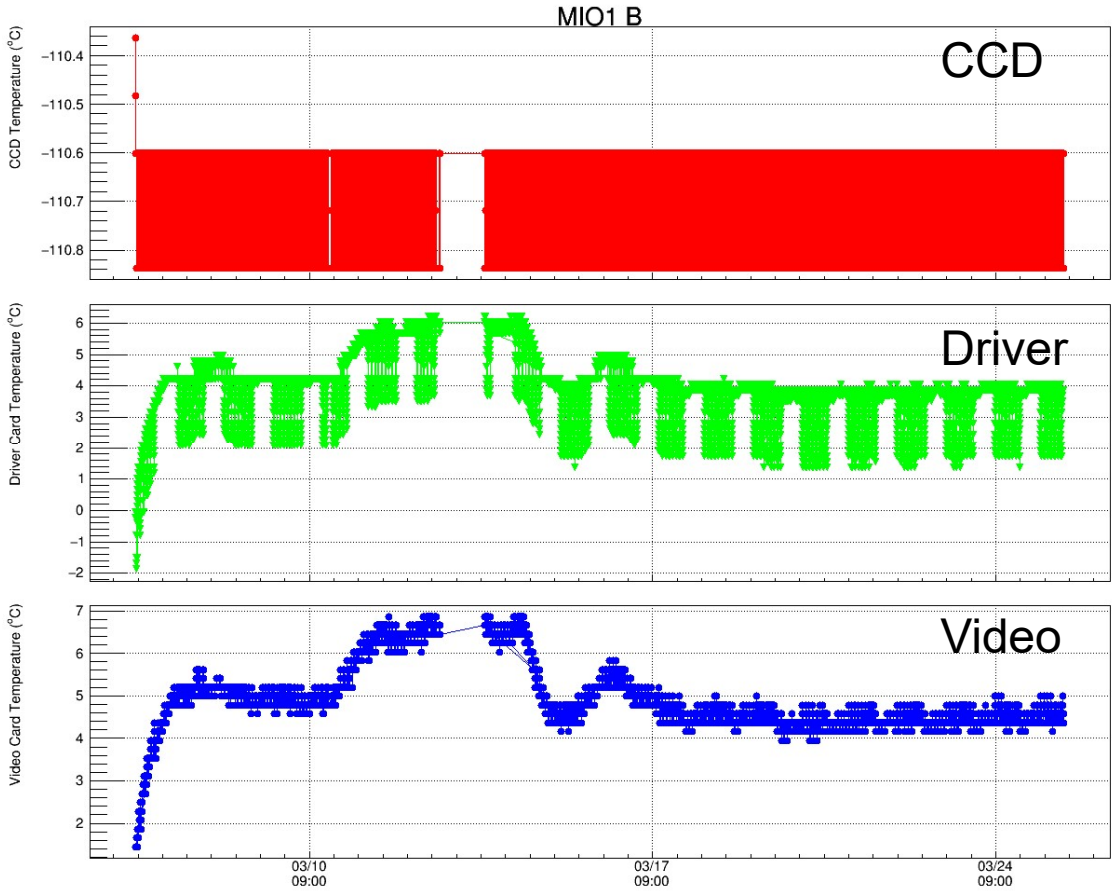
c.f. 2013 INL=0.28±0.02%



Temperature dependence of gain

- Temperature change of the Video Board on which ASIC is mounted affects the gain of the pre-amplifier circuit inside the chip
- Usage temperature range of SXI sensor is −20℃～+30℃ (T.B.D.)

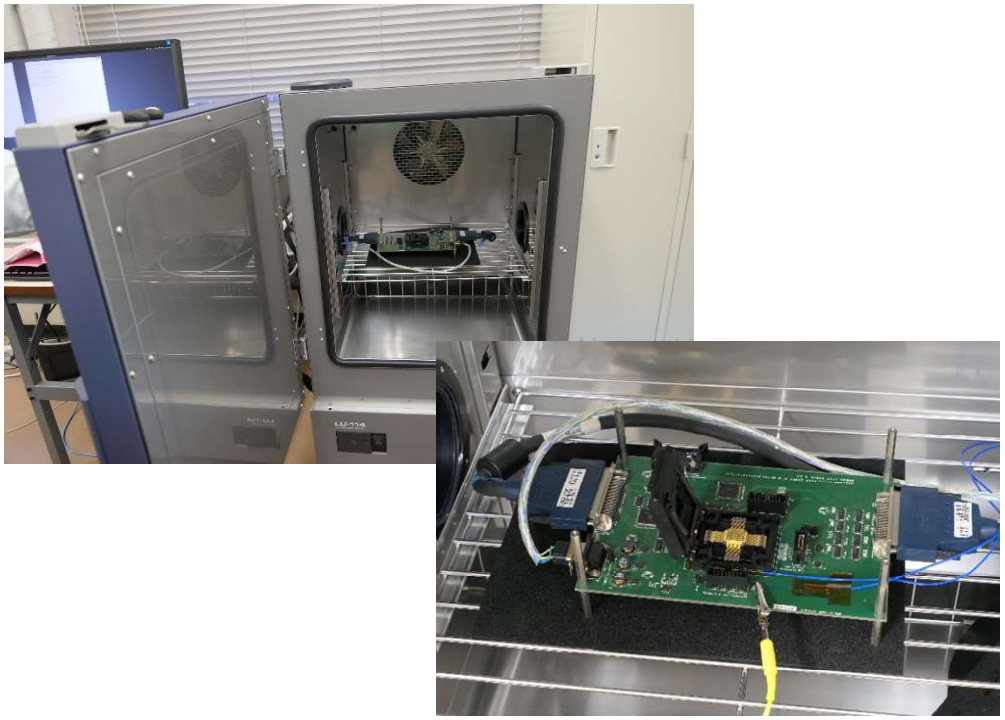
- Because the Hitomi data is not sufficient to investigate the dependence, we need to test chips that are chosen from the same lot as flight model chips on ground

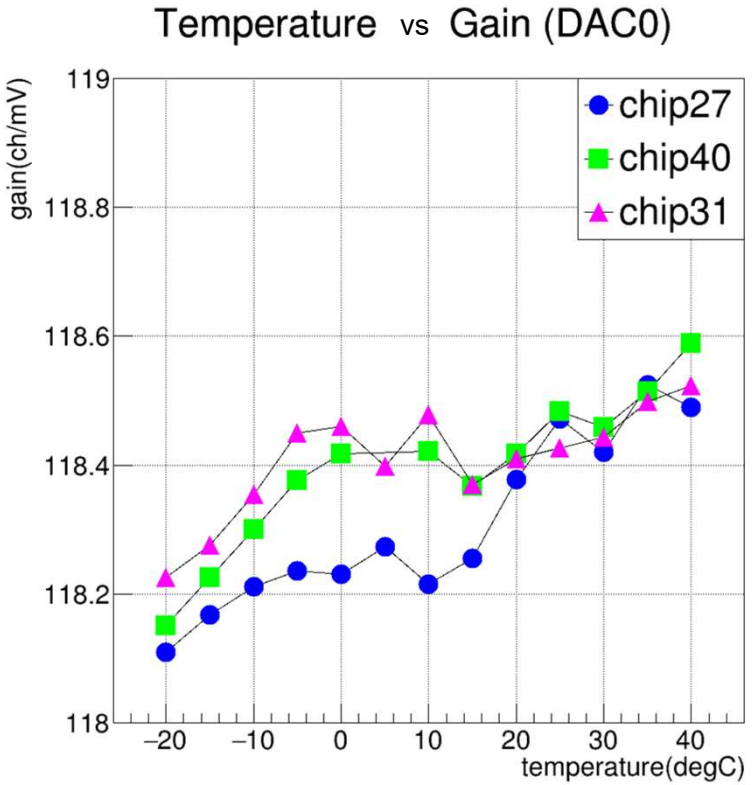


Temperature log of Hitomi/SXI

Gain calibration

- We performed calibration test with 3 chips among 23 using thermostatic chamber
- Slight change of the gain (0.1%/20℃) is observed for all chips, which will be included in CALDB





Summary

- We will reuse analog ASICs developed originally for Hitomi/SXI
  - Analog CCD signals are multiplied and digitized in the ASICs
  - Radiation tolerance has already been verified
- Some quality assurance tests were performed
  - Some chips were found to be discolored on the plated surface by visual inspection test
  - However, electrical performances have not significantly changed
  - Input equivalent noise of 33μV corresponds to noise level of 6.6e-
  - Effective energy range is confirmed to be 20.4keV
  - Temperature dependence of the gain is measured to be 0.1%/20℃
  - We will soon choose flight model chips and implement them on the Video Board